Programming the Flashlite 186 Watchdog Timer

The processor on the Flashlite 186 has a watchdog timer that can be enabled and then periodically reset to provide an automatic reset function.

Initial configuration

First of all, send 2 hex words of 0xAAAA and 0x5555 to the WDTCON register at I/O port 0xFFE6 in that order. This will reset the watchdog counter register.

Next, send 2 hex words of 0x3333 and 0xCCCC to the WDTCON register in that order. This will unlock the register so that it can receive a command.

Finally, send the enable command to the WDTCON register. This is of the form 0xC0nn where nn is equal to the watchdog timeout delay specified in this table:

0x01 30us. 0x02 31ms. 0x04 62ms. 0x08 125ms. 0x10 251ms. 0x20 503ms. 0x40 1 sec 0x80 2 sec

For example, a command to enable the watchdog timer with a 1 second timout would consist of sending a word of 0xC040 to 0xFFE6.

Periodic Watchdog Reset

To periodically reset the watchdog timer, send 2 hex words of 0xAAAA and 0x5555 to the WDTCON register at I/O port 0xFFE6 in that order.